Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A process for forming a chip structure with a resistor, comprising:
providing a semiconductor substrate;
forming a plurality of electronic devices and a resistor in a surface layer of the semiconductor substrate;
forming a plurality of dielectric layers and a plurality of circuit layers over the semiconductor substrate, the dielectric layers stacked over the semiconductor substrate, the dielectric layers having a plurality of via holes, each of the circuit layers disposed on corresponding one of the dielectric layers respectively, wherein the circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices;
forming a passivation layer over the dielectric layers and the circuit layers; and
forming a circuit line over the passivation layer, wherein the circuit line passes through the passivation layer to electrically connect the resistor to the circuit layers.

[c2] 2. The process as claimed in claim 1, wherein the resistor is formed by doping boron, phosphorous, arsenic or

gallium into the semiconductor substrate through the surface of the semiconductor.

[c3] 3. The process as claimed in claim 1, wherein the resistor is made of a material of constituting a N well, a P well, a N^+ diffusion region or a P^+ diffusion region.

[c4] 4. The process as claimed in claim 1, further comprising forming an insulation layer over the passivation layer and the insulation layer covering the circuit line.

[c5] 5. The process as claimed in claim 4, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c6] 6. The process as claimed in claim 1, further comprising forming an insulation layer between the passivation layer and the circuit line.

[c7] 7. The process as claimed in claim 6, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c8] 8. A process for forming a chip structure with a resistor, comprising:
providing a semiconductor substrate;

forming a plurality of electronic devices in a surface layer of the semiconductor substrate;

forming a plurality of dielectric layers, a plurality of circuit layers and a resistor over the semiconductor substrate, the dielectric layers stacked over the semiconductor substrate, the dielectric layers having a plurality of via holes, the resistor disposed on one of the dielectric layers, each of the circuit layers disposed on corresponding one of the dielectric layers respectively, wherein the circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices;

forming a passivation layer over the dielectric layers and the circuit layers; and

forming a circuit line over the passivation layer, wherein the circuit line passes through the passivation layer to electrically connect the resistor to the circuit layers.

[c9] 9. The process as claimed in claim 8, wherein the resistor is formed by depositing polysilicon using a chemical-vapor-deposition (CVD) process.

[c10] 10. The process as claimed in claim 8, wherein the resistor is formed by depositing polysilicon using a chemical-vapor-deposition (CVD) process and then doping boron, phosphorous, arsenic or gallium into the deposited polysilicon.

[c11] 11. The process as claimed in claim 8, wherein the resistor is formed by depositing aluminum, copper, tungsten, an aluminum alloy or a cooper alloy using a vapor-deposition process.

[c12] 12. The process as claimed in claim 8, further comprising forming an insulation layer over the passivation layer, the insulation layer covering the circuit line.

[c13] 13. The process as claimed in claim 12, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c14] 14. The process as claimed in claim 8, further comprising forming an insulation layer between the passivation layer and the circuit line.

[c15] 15. The process as claimed in claim 14, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c16] 16. A process for forming a chip structure with a resistor, comprising:
providing a semiconductor substrate;
forming a plurality of electronic devices in a surface layer

of the semiconductor substrate;

forming a plurality of dielectric layers and a plurality of circuit layers over the semiconductor substrate, the dielectric layers stacked over the semiconductor substrate, the dielectric layers having a plurality of via holes, each of the circuit layers disposed on corresponding one of the dielectric layers respectively, wherein the circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices;

forming a passivation layer over the dielectric layers and the circuit layers;

forming a resistor over the passivation layer by a depositing process; and

forming a circuit line over the passivation layer, wherein the circuit line passes through the passivation layer to electrically connect the resistor to the circuit layers.

[c17] 17. The process as claimed in claim 16, wherein the resistor is formed by depositing aluminum, an aluminum alloy, copper, a copper alloy, a nickel-chromium alloy, a nickel-tin alloy, tantalum nitride, tantalum or tungsten using a vapor-deposition method or an electroplating method.

[c18] 18. The process as claimed in claim 16, further comprising forming an insulation layer over the passivation

layer, the insulation layer covering the circuit line.

[c19] 19. The process as claimed in claim 18, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c20] 20. The process as claimed in claim 16, further comprising forming an insulation layer between the passivation layer and the circuit line.

[c21] 21. The process as claimed in claim 20, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c22] 22. A chip structure with a resistor, comprising:
a semiconductor substrate having a surface layer;
a plurality of electronic devices positioned in the surface layer of the semiconductor substrate;
a resistor positioned in the surface layer of the semiconductor substrate;
a plurality of dielectric layers stacked over the semiconductor substrate and the dielectric layers having a plurality of via holes;
a plurality of circuit layers each disposed on corresponding one of the dielectric layers respectively, wherein the

circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices;

a passivation layer positioned over the dielectric layers and the circuit layers; and

a circuit line positioned over the passivation layer, wherein the circuit line passes through the passivation layer to electrically connect the resistor to the circuit layers.

[c23] 23. The chip structure as claimed in claim 22, wherein a material constituting the resistor is silicon with a dopant selected from the group of boron, phosphorous, arsenic and gallium.

[c24] 24. The chip structure as claimed in claim 22, wherein the resistor is made of a material of constituting a N well, a P well, a N^+ diffusion region or a P^+ diffusion region.

[c25] 25. The chip structure as claimed in claim 22, further comprising an insulation layer positioned over the passivation layer and the insulation layer covering the circuit line.

[c26] 26. The chip structure as claimed in claim 25, wherein the material of constituting the insulation layer is made

of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c27] 27. The chip structure as claimed in claim 22, further comprising an insulation layer positioned between the passivation layer and the circuit line.

[c28] 28. The chip structure as claimed in claim 27, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c29] 29. A chip structure with a resistor, comprising:
a semiconductor substrate;
a plurality of electronic devices positioned in a surface layer of the semiconductor substrate;
a plurality of dielectric layers stacked over the semiconductor substrate and the dielectric layers having a plurality of via holes;
a plurality of circuit layers each disposed on corresponding one of the dielectric layers respectively, wherein the circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices;
a resistor positioned on one of the dielectric layers;

a passivation layer positioned over the dielectric layers and the circuit layers; and

a circuit line positioned over the passivation layer, wherein the circuit line passes through the passivation layer to electrically connect the resistor to the circuit layers.

[c30] 30. The chip structure as claimed in claim 29, wherein a material of constituting the resistor is polysilicon.

[c31] 31. The chip structure as claimed in claim 29, wherein a material of constituting the resistor is polysilicon with a dopant selected from the group of boron, phosphorous, arsenic and gallium.

[c32] 32. The chip structure as claimed in claim 29, wherein a material constituting the resistor is aluminum, copper, tungsten, an aluminum alloy or a copper alloy.

[c33] 33. The chip structure as claimed in claim 29, further comprising an insulation layer positioned over the passivation layer and the insulation layer covering the circuit line.

[c34] 34. The chip structure as claimed in claim 33, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric ma-

terial.

[c35] 35. The chip structure as claimed in claim 29, further comprising an insulation layer positioned between the passivation layer and the circuit line.

[c36] 36. The chip structure as claimed in claim 35, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c37] 37. A chip structure with a resistor, comprising:
a semiconductor substrate;
a plurality of electronic devices positioned in a surface layer of the semiconductor substrate;
a plurality of dielectric layers stacked over the semiconductor substrate and the dielectric layers having a plurality of via holes;
a plurality of circuit layers each disposed on corresponding one of the dielectric layers respectively, wherein the circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices;
a passivation layer positioned over the dielectric layers and the circuit layers; and
a resistor formed by a depositing process and positioned

over the passivation layer; and
a circuit line positioned over the passivation layer, wherein the circuit line passes through the passivation layer to electrically connect the resistor to the circuit layers.

[c38] 38. The chip structure as claimed in claim 37, wherein a material constituting the resistor is aluminum, an aluminum alloy, copper, a copper alloy, a nickel-chromium alloy, a nickel-tin alloy, tantalum nitride, tantalum or tungsten.

[c39] 39. The chip structure as claimed in claim 37, further comprising an insulation layer positioned over the passivation layer and the insulation layer covering the circuit line.

[c40] 40. The chip structure as claimed in claim 39, wherein the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.

[c41] 41. The chip structure as claimed in claim 37, further comprising an insulation layer positioned between the passivation layer and the circuit line.

[c42] 42. The chip structure as claimed in claim 41, wherein

the material of constituting the insulation layer is made of polyimide (PI), benzocyclobutene (BCB), porous dielectric material, parylene, elastomer or low k dielectric material.